an addressing circuit which enables the combined subpixel outputs stored on said pixel's intrinsic capacitance to be read out in response to an address input.

REMARKS

This amendment is in response to the Final Office Action dated 3/11/03. The amendment accompanies a Request for Continued Examination (RCE) filed in accordance with 37 C.F.R. 1.114. Entry of this Amendment and reconsideration of this application are respectfully requested. Please note that the amended claims are reproduced completely without indication of insertions or deletions. The amendments are also given in the older format, with insertions and deletions, in Attachment A following these remarks.

Claim Rejections under 35 U.S.C. §103

Claims 1, 5, 9 and 13-15

Claims 1, 5, 9 and 13-15 were rejected as obvious over a patent to Arques et al. in view of a patent to Wilder et al., and further in view of Takahashi.

A brief review of the prosecution history is in order. In the Examiner's previous Office Action, this same group of claims was rejected as obvious over Arques in view of Wilder. In response, applicant presented amendments and arguments respecting claims 1 and 9. The present Office Action now arrives, noting that "applicant's arguments with respect to claims 1, 5, 9 and 13-15 have been considered but are moot in view of the new ground(s) of rejection." This implies that the applicant's response was persuasive with respect to Arques and Wilder, but that the patent to Takahashi - the "new grounds" of rejection - renders the claims obvious once again. Therefore, the discussion below largely focuses on Takahashi and its relevance to the

claims at issue.

Claim 1

Claim 1 is directed to a photodetector array comprising a plurality of addressable active pixels. Each pixel in the array must comprise:

- at least two photodiodes arranged such that their outputs may be switchably connected to a common pixel node;

- a switching circuit which allows switching of at least one of the photodiodes between a first circuit and a second circuit, wherein the first circuit directly combines the outputs of said at least two photodiodes in parallel, and the second circuit directly combines the output of the at least one photodiode in parallel with the output of a photodiode of a neighboring pixel in the array;

- such that the array is switchable between a high resolution and a low resolution pixel configuration, the pixel having an intrinsic capacitance which stores the combined photodiode outputs prior to their being read out, and

- an addressing circuit which enables the combined photodiode outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

Thus, as amended, each pixel in the claimed photodetector array is an active pixel, which includes at least two photodiodes which are capable of being switched to a common pixel node (support for these amendments can be found with reference to FIGs. 2a and 2b). An array of "active" pixels is one which includes an amplifier for each pixel.

In addition, the array includes a switching circuit arranged so that:

- the outputs of the at least two photodiodes making up a pixel can be combined in parallel, or

- the output of at least one of the pixel's two photodiodes can be combined with the output of a photodiode of a neighboring pixel.

Each pixel in an array is "read out" to determine the amount of light which has impinged on the pixel. Claim 1 requires that the photodetector outputs be combined directly, prior to the pixel's being read out. This means that the photodetector outputs themselves must be connected together ("combined") before the pixel is read out.

The cited art is quite different. The patent to Arques has almost no relevance whatsoever to the claims in question. Arques does disclose a pixel with two diodes, but this is the only similarity between the claimed array and Arques.

Arques discloses an array of passive pixels (i.e., no local amplifiers), each of which has one photosensitive diode and one reading diode (Abstract). Arques needs the second diode in order to read what he calls "the photosensitive dots". In this sense, the second diode is part of the readout circuitry and not related to the charge accumulation operation of the photodiode. The task of the second diode is to prevent the charge on the photosensitive dot from leaking out when reading other pixels in the same column. The two photodiodes in Arques' patent are connected in series with opposite directions of conduction (see title and FIG. 1 of his patent). This is required in order to perform the function he is describing: using the two diodes to read a specific photosensitive dot within a large array of pixels.

In all of these particulars, Arques differs radically from what is recited in claim 1. In claim 1, all of the recited photodiodes may be involved in the charge accumulation operation; none of the photodiodes could be considered to be part of the

readout circuitry.

In addition, claim 1 requires that the "at least two photodiodes [be] arranged such that their outputs are switchably connected to a common pixel node". See, for example, FIG. 2a, where the cathodes of photodiodes PD1 and PD2 in pixel 30 may both be connected to a common pixel node (by closing switch S1), and the cathodes of photodiodes PD3 and PD4 in pixel 32 may both be connected to a different common pixel node (by closing switch S3).

The arrangement in Arques is very different. As noted in Arques' Abstract, each of his pixels consists of a photosensitive diode and a reading diode, connected in series between a row and a column of the matrix. As such, there is no way to connect the outputs of his diodes to a common pixel node - as is required in claim 1.

Nor does Arques disclose anything remotely resembling the switching circuit and addressing circuit elements of claim 1. Arques says nothing about a means for "directly combining the outputs of said at least two photodiodes in parallel", or a means for "directly combining the output of the at least one photodiode in parallel with the output of a photodiode of a neighboring pixel in the array" - as is required in claim 1. In fact, Arques says nothing about combining photodiode outputs in various combinations.

Nor does Arques disclose an array which is switchable between a high resolution and a low resolution pixel configuration, or an addressing circuit which enables the combined photodiode outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

Thus, Arques fails to disclose the following elements of claim 1:

- an array of active pixels;

- at least two photodiodes arranged such that their outputs may be switchably connected to a common pixel node;

- a switching circuit which allows switching of at least one of the photodiodes between a first circuit and a second circuit; wherein the first circuit directly combines the outputs of the at least two photodiodes in parallel, and the second circuit directly combines the output of the at least one of the photodiodes in parallel with the output of a photodiode of a neighboring pixel in the array, whereby the array is switchable between a high resolution and a low resolution pixel configuration, the pixel having an intrinsic capacitance which stores the combined photodiode outputs prior to their being read out, and

- an addressing circuit which enables the combined photodiode outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

In other words, the only property common to both claim 1 and Arques is the presence of 2 diodes. But the type of diodes, the way the diodes are connected, and the purpose and usage of the diodes are totally different - rendering the Arques patent largely irrelevant to the claims at issue.

With respect to Wilder: Wilder discusses pixel addressing, but says nothing about combining photodiode outputs to achieve various pixel resolution configurations.

It must first be noted that Wilder never even mentions photodiodes; his system is discussed at the pixel level only. This is in contrast to the applicant's invention, which focuses on the photodiode or photodiodes that make up each pixel. As noted above, claim 1 requires that the photodetector outputs be combined directly, which requires that the photodetector outputs be connected together before the pixel is read out. Because

Wilder operates at the pixel level, he cannot and does not combine photodetector outputs prior to the pixel's being read out.

As such, Wilder cannot and does not disclose:

- a switching circuit which allows switching of at least one of the photodiodes between a first circuit and a second circuit, wherein the first circuit directly combines the outputs of said at least two photodiodes in parallel, and the second circuit directly combines the output of the at least one photodiode in parallel with the output of a photodiode of a neighboring pixel in the array; nor

- an addressing circuit which enables the combined photodiode outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

Wilder's patent describes a way to achieve xy-addressability, but only for passive pixels; i.e., for pixels which lack a local amplifier. Simply, the charge on a pixel is read and then amplified externally; as such, it is very simple to change the resolution because one need only select more than one pixel at a time, and the charge of all selected pixels gets added on the read bus line or the external readout capacitor.

In contrast, the applicant's claim 1 recites an array of active pixels, with an amplifier for every pixel. The invention enables the effective resolution to be changed by connecting or isolating photodiodes before each pixel's readout amplifier.

To summarize, the combination of Arques and Wilder fails to disclose the following elements of claim 1:

- an array of active pixels;

- at least two photodiodes arranged such that their outputs may be switchably connected to a common pixel node;

- a switching circuit which allows switching of at least one

of the photodiodes between a first circuit and a second circuit; wherein the first circuit directly combines the outputs of the at least two photodiodes in parallel, and the second circuit directly combines the output of the at least one of the photodiodes in parallel with the output of a photodiode of a neighboring pixel in the array, whereby the array is switchable between a high resolution and a low resolution pixel configuration, the pixel having an intrinsic capacitance which stores the combined photodiode outputs prior to their being read out, and

- an addressing circuit which enables the combined photodiode outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

Takahashi

Now the Examiner turns to Takahashi to make up for the above-noted shortcomings of Arques and Wilder. Takahashi fails to do so, as discussed below.

The Examiner refers applicant to FIG. 8, #24 and #6 of Takahashi. It is not clear why this is: #24 is a photodiode and #6 is a switching transistor, which do nothing to meet the requirements of claim 1 as presently constituted.

Please refer to Takahashi's FIG. 2, which illustrates exactly how it is that he combines pixel outputs. As is clearly shown in FIG. 2, Takahashi fabricates a device in which two pixels (one on the left side of region 21 and one on the right side of region 21) are connected together at a "floating diffusion" (FD) region 21. It is here at n^+ FD region 21 that the two pixel outputs may be combined. As a result of this very specific fabrication scheme, the only possible combinations Takahashi can provide are one pixel output, or two pixel outputs - with the two pixels restricted to those connected together via

FD region 21. No other combinations are possible - Takahashi's FD approach is inherently limited thusly.

As such, Takahashi cannot and does not provide the missing elements of claim 1. In accordance with claim 1:

a) each active pixel must contain at least 2 photodiodes which can be switchably connected to a common pixel node;

b) a switching circuit must enable the direct combination of the at least 2 photodiodes making up a pixel; OR

c) the switching circuit must enable the direct combination of at least one of the pixel's at least two photodiodes with the output of a photodiode of a neighboring pixel.

Takahashi fails to disclose any of these elements.

With respect to element "a":

In all of Takahashi's embodiments, he employs one photodiode in each pixel - see, e.g., column 3, lines 49-55, which states that FIG. 1 shows a sensor of 2 columns by 4 rows; each of the eight pixels includes one photodiode. As such, claim 1's requirement that each pixel contain "at least two photodiodes arranged such that their outputs may be switchably connected to a common pixel node" is not met. Takahashi does show more than one photodiode being switchably connected to a common pixel node - e.g., photodiodes 1 in pixel 30-11 and 30-21 in FIG. 1 are switchably connected to node 21. But these photodiodes are <u>not</u> in the same pixel. Element "a" is not met.

With respect to element "b":

Takahashi fails to disclose any means of directly combining the at least 2 photodiodes making up a pixel. It is physically impossible for Takahashi to do this, as he has no pixels

containing at least 2 photodiodes. Takahashi does disclose combining the outputs of 2 photodiodes, but his photodiodes are in different pixels. This is not what claim 1 requires. Element "b" is not met.

With respect to element "c":

Takahashi fails to disclose any means of enabling the direct combination of at least one of the pixel's at least two photodiodes with the output of a photodiode of a neighboring pixel. This element again requires the presence of at least 2 photodiodes in a pixel. Takahashi fails to disclose this, and this element "c" is not met.

Further, elements "b" and "c" require two different combinations of at least two photodiodes. As noted above, Takahashi can only provide one such combination - it is physically impossible for his device to provide more that one combination of two photodiodes. Takahashi simply does not provide the means to provide the combinations specified in both elements b and c.

In addition, Takahashi fails to disclose an array which "is switchable between a high resolution and a low resolution pixel configuration" - as is required by claim 1. Takahashi's patent says nothing about providing a selectable pixel resolution. As described at, e.g., column 2, lines 37-56, Takahashi's approach is designed to reduce the physical size of his image sensor, by having each source-follower MOS amplifier be shared by more than one pixel. Takahashi fails to disclose or suggest the providing of a selectable pixel resolution, and provides no means of achieving this functionality.

It should further be noted that Takahashi's FD approach

takes up space in his device; the applicant's device, which does not require a FD region, does not consume this space. In addition, Takahashi's performance can be degraded by combining pixel outputs using a FD region, due to signal losses that can arise from charge sharing between the photodiode and FD regions.

Thus, Takahashi completely fails to overcome the shortcomings of Arques and Wilder. The missing elements and functionality are critical to the intended (and claimed) function of the applicant's design - i.e., that of providing a selectable pixel resolution.

To summarize, the combination of Arques, Wilder and Takahashi fails to disclose the following elements of claim 1:

- an array of active pixels, each of which includes at least two photodiodes arranged such that their outputs may be switchably connected to a common pixel node;

- a switching circuit which allows switching of at least one of the photodiodes between a first circuit and a second circuit; wherein the first circuit directly combines the outputs of the at least two photodiodes in parallel, and the second circuit directly combines the output of the at least one of the photodiodes in parallel with the output of a photodiode of a neighboring pixel in the array, whereby the array is switchable between a high resolution and a low resolution pixel configuration, the pixel having an intrinsic capacitance which stores the combined photodiode outputs prior to their being read out, and

- an addressing circuit which enables the combined photodiode outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

Thus, virtually none of the elements of claim 1 are disclosed by the cited art - either alone or in combination.

Even if combined as suggested, the resulting system would differ radically from the claimed array, in both structure and function.

Not that there is any suggestion to combine the cited references. The Examiner cites no teachings or suggestions which suggest his combination. He does mention the existence of "motivation" to combine, but when it is considered that not one of the three references being combined even hints at the concept of providing a selectable resolution, any such motivation is difficult to discern. And it is well-established that lacking any teaching, suggestion or motivation, it is improper to combine references to establish obviousness.

As Arques, Wilder and Takahashi lack the above-noted essential elements of claim 1,

as their combination would not result in the claimed invention, and

as there is no clear motivation to combine as suggested,

it is improper to find that claim 1 is obvious in view of them. Claim 1 is therefore allowable over Arques, Wilder and Takahashi.

Claim 5

Claim 1 is the parent of claim 5, which is therefore allowable along with claim 1.

Claim 9

Claim 9 is an independent claim directed to a photodetector array. Claim 9 has been amended to better clarify its differences with respect to the cited art. As amended, claim 9 recites a photodetector array with selectable resolution, which comprises:

- a plurality of photodetectors;
- a switching circuit which configures neighboring photodetectors into active pixels by directly summing at each pixel the outputs of multiple photodetectors into an aggregated pixel output, the photodetector outputs summed at each pixel arranged such that their outputs are switchably connected to a common pixel node, the aggregated pixel output stored on the pixel's intrinsic capacitance prior to being read out;
- wherein the switching circuit is electronically switchable to aggregate the photodetector signals according to at least two different selectable pixellization schemes with differing resolutions, such that the switching circuit combines photodetector signals according to at least two different, electronically selectable configurations:

- a first configuration in which each pixel output is a sum of the outputs of two neighboring photodiodes from within a single pixel; and

- a second configuration in which each pixel output is a sum of at least three photodiodes; and
- a plurality of addressable interface circuits, each of which enables the aggregated pixel output stored on a respective one of the pixel's to be read out in response to an address input.

Thus, each pixel in the claimed photodetector array is an active pixel, formed by aggregating photodetectors such that their outputs are summed together at a common pixel node.

In addition, the array is arranged so that:
- the switching circuit is electronically switchable between at least two different pixellization schemes with differing resolutions:

a first configuration in which each pixel output is a sum of the outputs of two neighboring photodiodes from within a single pixel; and

a second configuration in which each pixel output is a sum of at least three photodiodes.

As noted above, the cited art is quite different.

Arques discloses an array of passive pixels, made up of first and second diodes, with the second diode being part of the readout circuitry and not related to the charge accumulation operation of the photodiode.

Furthermore, the two photodiodes in Arques' patent are connected in series with opposite directions of conduction. This is required in order to perform the function he is describing: using the two diodes to read a specific photosensitive dot within a large array of pixels.

In all of these particulars, Arques differs radically from what is recited in the amended claim 9. In claim 9, all of the recited photodetectors may be involved in the charge accumulation operation; none of the photodetectors could be considered to be part of the readout circuitry.

In addition, claim 9 requires that the photodetector outputs summed at each pixel are arranged such that their outputs are switchably connected to a common pixel node; this arrangement is shown, for example, in FIG. 2a, where the cathodes of photodiodes PD1 and PD2 in pixel 30 may both be connected to a common pixel node (by closing switch S1), and the cathodes of photodiodes PD3 and PD4 in pixel 32 may both be connected to a different common pixel node (by closing switch S3).

The arrangement in Arques is very different: each of his pixels consists of a photosensitive diode and a reading diode, connected in series between a row and a column of the matrix. As such, there is no way to connect the outputs of his diodes to a common pixel node in the manner specified in the amended claim 9.

Nor does Arques disclose anything remotely resembling the switching circuit and addressing circuit elements of claim 9. Arques says nothing about a means for providing "at least two different, electronically selectable configurations: a first configuration in which each pixel output is a sum of the outputs of two neighboring photodiodes from within a single pixel; and a second configuration in which each pixel output is a sum of at least three photodiodes" - as is required in claim 9. In fact, Arques says nothing about combining photodiode outputs in various combinations.

Nor does Arques disclose an addressing circuit which enables the combined photodiode outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

Thus, Arques fails to disclose the following elements of the amended claim 9:

- a switching circuit which configures neighboring photodetectors into active pixels by directly summing at each pixel the outputs of multiple photodetectors into an aggregated pixel output;

- photodetector outputs summed at each pixel arranged such that their outputs are switchably connected to a common pixel node;

- wherein the switching circuit is electronically switchable to aggregate the photodetector signals according to at least two different selectable pixellization schemes with differing resolutions, such that the switching circuit combines photodetector signals according to at least two different, electronically selectable configurations: a first configuration in which each pixel output is a sum of the outputs of two neighboring photodiodes from within a single pixel; and a second

configuration in which each pixel output is a sum of at least three photodiodes.

In other words, both claim 9 and Arques require the use of multiple diodes. But the type of diodes, the way the diodes are connected, and the purpose and usage of the diodes are totally different - rendering the Arques patent largely irrelevant to the amended claim 9.

The patent to Wilder does nothing to cure the deficiencies in Arques. Wilder discusses pixel addressing, but says nothing about combining photodiode outputs to achieve various pixel resolution configurations. Wilder never even mentions photodiodes; his system is discussed at the pixel level only. This is in contrast to the applicant's invention, which focuses on the photodiode or photodiodes that make up each pixel. As such, Wilder cannot and does not disclose:

- a switching circuit which is electronically switchable to aggregate the photodetector signals according to at least two different selectable pixellization schemes with differing resolutions, such that the switching circuit combines photodetector signals according to at least two different, electronically selectable configurations: a first configuration in which each pixel output is a sum of the outputs of two neighboring photodiodes from within a single pixel; and a second configuration in which each pixel output is a sum of at least three photodiodes; and

- a plurality of addressable interface circuits, each of which enables the aggregated pixel output stored on a respective one of the pixel's to be read out in response to an address input.

Wilder's patent describes a way to achieve xy-

addressability, but only for passive pixels. In contrast, the applicant's claim 9 recites an array of active pixels, with an amplifier for every pixel. The invention enables the effective resolution to be changed by connecting or isolating photodiodes before each pixel's readout amplifier.

Takahashi

As with claim 1, the patent to Takahashi fails to make up for the above-noted shortcomings of Arques and Wilder with respect to claim 9. Again, there are substantial differences which render a finding of obviousness improper in this case.

In accordance with claim 9 -

a) the switching circuit must be electronically switchable to aggregate the photodetector signals according to at least two different selectable pixellization schemes with differing resolutions,

b) such that the switching circuit combines photodetector signals according to at least two different, electronically selectable configurations:

- a first configuration in which each pixel output is a sum of the outputs of two neighboring photodiodes from within a single pixel; and

- a second configuration in which each pixel output is a sum of at least three photodiodes.

Takahashi fails to disclose these elements of the amended claim 9.

With respect to element "a":

Takahashi fails to disclose an array which is "electronically switchable to aggregate the photodetector signals according to at least two different selectable pixellization

schemes with differing resolutions" - as is required by claim 9. Takahashi's patent says nothing about providing a selectable pixel resolution. As described at, e.g., column 2, lines 37-56, Takahashi's approach is designed to reduce the physical size of his image sensor, by having each source-follower MOS amplifier be shared by more than one pixel. Takahashi fails to disclose or suggest the providing of a selectable pixel resolution, and provides no means of achieving this functionality.

With respect to element "b":

In all of Takahashi's embodiments, he employs one photodiode in each pixel - see, e.g., column 3, lines 49-55, which states that FIG. 1 shows a sensor of 2 columns by 4 rows; each of the eight pixels includes one photodiode. As such, claim 9's requirement that each pixel output "is a sum of the outputs of two neighboring photodiodes from within a single pixel" is not met. Takahashi does show more than one photodiode being switchably connected to a common pixel node - e.g., photodiodes 1 in pixel 30-11 and 30-21 in FIG. 1 are switchably connected to node 21. But these photodiodes are not in the same pixel. Element "b" is not met.

Further, element "b" require two different combinations of at least two photodiodes: a first combination which sums the outputs of two neighboring photodiodes, and a second combination which sums the outputs of three photodiodes. As noted above, Takahashi can only provide one such combination: it is physically impossible for his device to provide more that one combination of two photodiodes, and he provides NO combinations of three photodiodes. Takahashi simply does not provide the means to provide the combinations specified in element b.

Thus, Takahashi again fails to overcome the shortcomings of

Arques and Wilder with respect to the amended claim 9. The missing elements and functionality are critical to the intended (and claimed) function of the applicant's design - i.e., that of providing a selectable pixel resolution.

In sum, then, virtually none of the elements of the amended claim 9 are disclosed by the cited art - either alone or in combination. Even if combined as suggested, the resulting system would be significantly different from the claimed array in both structure and function.

Applicant again wishes to note that the Examiner cites no teachings or suggestions which suggest the combination of references used to reject claim 9, and that any alleged motivation to combine is difficult to discern. And it is well-established that lacking any teaching, suggestion or motivation, it is improper to combine references to establish obviousness.

As Arques, Wilder and Takahashi lack the above-noted essential elements of the amended claim 9,

as their combination would not result in the claimed invention, and

as there is no clear motivation to combine as suggested,

it is improper to find that claim 9 is obvious in view of them. The amended claim 9 is therefore allowable over Arques, Wilder and Takahashi.

Claim 15

Claim 15 is an independent claim directed to a photodetector array. Claim 15 has been amended to better clarify its differences with respect to the cited art. As amended, claim 15 recites a photodetector array, comprising a plurality of active pixels comprising a plurality of pixels arranged into at least

three horizontal rows and vertical columns,
- wherein each pixel comprises an association of at least two subpixels arranged such that their outputs may be switchably connected to a common pixel node;
- and wherein the outputs of the subpixels are switchably combined into at least two different grouping arrangements, to give at least two different selectable pixel resolutions, wherein the at least two different grouping arrangements comprises two different grouping arrangements, one of which combines the outputs of two adjacent subpixels in a given vertical column, and the other of which combines the outputs of three adjacent subpixels in the given vertical column,
- each of the pixels having an intrinsic capacitance which stores the combined subpixel outputs prior to their being read out, and
- an addressing circuit which enables the combined subpixel outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

As above, the patent to Arques is largely irrelevant to claim 15. Arques fails to disclose the following elements of claim 15:

- an array of active pixels arranged into at least three horizontal rows and vertical columns;

- pixels which comprise at least two subpixels arranged such that their outputs may be switchably connected to a common pixel node;

- wherein the outputs of the subpixels are switchably combined into at least two different grouping arrangements to give at least two different selectable pixel resolutions, one of which combines the outputs of two adjacent subpixels in a given vertical column, and the other of which combines the outputs of three adjacent subpixels in the given vertical column.

As before, the patent to Wilder does nothing to cure the deficiencies in Arques. Wilder says nothing about combining subpixel outputs to achieve various pixel resolution configurations. As such, Wilder cannot and does not disclose:

- switchably combining the outputs of the subpixels into at least two different grouping arrangements, to give at least two different selectable pixel resolutions, wherein the at least two different grouping arrangements comprises two different grouping arrangements, one of which combines the outputs of two adjacent subpixels in a given vertical column, and the other of which combines the outputs of three adjacent subpixels in the given vertical column, and
- an addressing circuit which enables the combined subpixel outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

In sum, then, virtually none of the elements of claim 15 are disclosed by the cited art - either alone or in combination. Even if combined as suggested, the resulting system would be significantly different from the claimed array in both structure and function.

Takahashi

As with claims 1 and 9, the patent to Takahashi fails to make up for the above-noted shortcomings of Arques and Wilder. Again, there are substantial differences which render a finding of obviousness improper in this case.

In accordance with claim 15 -

a) each pixel comprises an association of at least two subpixels arranged such that their outputs may be switchably connected to a common pixel node; and

b) the outputs of the subpixels are switchably combined into

at least two different grouping arrangements, to give at least two different selectable pixel resolutions, wherein the at least two different grouping arrangements comprises two different grouping arrangements, one of which combines the outputs of two adjacent subpixels in a given vertical column, and the other of which combines the outputs of three adjacent subpixels in the given vertical column.

Takahashi fails to disclose these elements of the amended claim 15.

With respect to element "a":

In all of Takahashi's embodiments, he employs one photodiode in each pixel - see, e.g., column 3, lines 49-55, which states that FIG. 1 shows a sensor of 2 columns by 4 rows; each of the eight pixels includes one photodiode. As such, claim 15's requirement that each pixel "comprise an association of at least two subpixels arranged such that their outputs may be switchably connected to a common pixel node" is not met. Takahashi does show more than one photodiode being switchably connected to a common pixel node - e.g., photodiodes 1 in pixel 30-11 and 30-21 in FIG. 1 are switchably connected to node 21. But these photodiodes are not in the same pixel. Element "a" is not met.

With respect to element "b":

Takahashi fails to disclose an array in which "the outputs of the subpixels are switchably combined into at least two different grouping arrangements, to give at least two different selectable pixel resolutions" - as is required by the amended claim 15. Takahashi's patent says nothing about providing a selectable pixel resolution. As described at, e.g., column 2, lines 37-56, Takahashi's approach is designed to reduce the physical size of his image sensor, by having each source-follower

MOS amplifier be shared by more than one pixel. Takahashi fails to disclose or suggest the providing of a selectable pixel resolution, and provides no means of achieving this functionality.

Further, element "b" require two different combinations: a first combination which combines the outputs of two adjacent subpixels in a given vertical column, and a second combination which combines the outputs of three adjacent subpixels in the given vertical column.

As noted above, Takahashi can only provide one such combination: it is physically impossible for his device to provide more that one combination of two photodiodes, and he provides NO combinations of three photodiodes. Takahashi simply does not provide the means to provide the combinations specified in element b.

Thus, Takahashi fails to overcome the shortcomings of Arques and Wilder with respect to the amended claim 15. The missing elements and functionality are critical to the intended (and claimed) function of the applicant's design - i.e., that of providing a selectable pixel resolution.

In sum, then, virtually none of the elements of the amended claim 15 are disclosed by the cited art - either alone or in combination. Even if combined as suggested, the resulting system would be significantly different from the claimed array in both structure and function.

Applicant again notes that the Examiner cites no teachings or suggestions which suggest the combination of references used to reject claim 15, and that any alleged motivation to combine is difficult to discern. And it is well-established that lacking

any teaching, suggestion or motivation, it is improper to combine references to establish obviousness.

As Arques, Wilder and Takahashi lack the above-noted essential elements of the amended claim 15,

as their combination would not result in the claimed invention, and

as there is no clear motivation to combine as suggested,

it is improper to find that claim 15 is obvious in view of them. The amended claim 15 is therefore allowable over Arques, Wilder and Takahashi.

Claim 13-14

Claim 15 is the parent of claims 13-14, which are therefore allowable along with claim 15.

Claims 2 and 3 were rejected as obvious over Arques, Wilder, and Takahashi in combination with a patent to Orava et al.

Claim 1 is the parent of claims 2 and 3, which are therefore allowable along with claim 1.

Claims 9 and 15 have been amended to overcome their rejection under §103. All of the claims presently in the application are believed to be in proper form for allowance. A Notice of Allowance is respectfully requested.

Respectfully submitted,

June 9, 2003

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Attachment A:

Amended claims with insertions and deletions indicated.

9. (thrice amended) A photodetector array with selectable resolution, comprising:

a plurality of photodetectors;

a switching circuit which configures neighboring ones of said photodetectors into active pixels by directly summing at each pixel the outputs of multiple photodetectors into an aggregated pixel output, said photodetector outputs summed at each pixel arranged such that their outputs are switchably connected to a common pixel node, said aggregated pixel output stored on said pixel's intrinsic capacitance prior to being read out;

wherein said switching circuit is electronically switchable to aggregate said photodetector signals according to at least two different selectable pixellization schemes with differing resolutions, such that said switching circuit combines photodetector signals according to at least two different, electronically selectable configurations: a first configuration in which each pixel output is a sum of the outputs of two neighboring photodiodes from within a single pixel; and a second configuration in which each pixel output is a sum of at least three photodiodes; and

a plurality of addressable interface circuits, each of which enables the aggregated pixel output stored on a respective one of said pixel's to be read out in response to an address input.

15. (thrice amended) A photodetector array, comprising a plurality of active pixels, said array of pixels comprising a plurality of pixels arranged into at least three horizontal rows and vertical columns,

wherein each pixel comprises an association of at least two subpixels arranged such that their outputs may be switchably connected to a common pixel node;

and wherein the outputs of said subpixels are switchably combined into at least two different grouping arrangements, to give at least two different selectable pixel [configurations] resolutions, wherein said at least two different grouping arrangements comprises two different grouping arrangements, one of which combines the outputs of two adjacent subpixels in a given vertical column, and the other of which combines the outputs of three adjacent subpixels in said given vertical column,

each of said pixels having an intrinsic capacitance which stores said combined subpixel outputs prior to their being read out, and

an addressing circuit which enables the combined subpixel outputs stored on said pixel's intrinsic capacitance to be read out in response to an address input.